Thermal Test Chip Packaging

Any semiconductor chip, whether it's a thermal test chip or an application device, is of no use unless it can be connected to, physically handled, and mounted in some reliable way. The purpose of semiconductor packaging is to provide these capabilities. However, there are many considerations that need to be addressed in selecting a chip package.

First is the issue of what type of chip needs to be packaged. The two types are wire bond (WB) and flip chip (FC). The latter is commonly referred to as bumped chip. In the former type, the chip has to be first mounted into a package and then connected to with wires – hence the name *Wire Bond* type. These are two separate operations and require specialized machinery to perform each operation. Many decisions have to be made in implementing these operations. For example, the kind of material that will be used to attach the chip to the package mounting area (referred to as die attachment material) is dependent on electrical, thermal, reliability and cost requirements. The material used for the wire bond, usually aluminum or gold wire, also has the similar requirements.

In FC packaging, the mounting of the chip and the electrical connection to the chip are performed as one operation. The package has to be designed with small solder pads to match the size and location of the bumps on the chip. The chip is physically placed onto the package and then the chip/package combination is heated to a temperature to cause the solder bumps on the chip to reflow onto the pads. Careful design and process control is required to make sure the solder does not connect to adjacent pads to avoid electrical shorting between pads and to make sure each of the chip bumps are properly attached. Once the attachment process is complete, an underfill operation is performed to inject epoxy-type material in the void area between the bumps. This helps to insure that the mounting is rugged and will minimize the effects of mechanical stress on the bumps as the chip heats up and/or the environmental temperature changes.

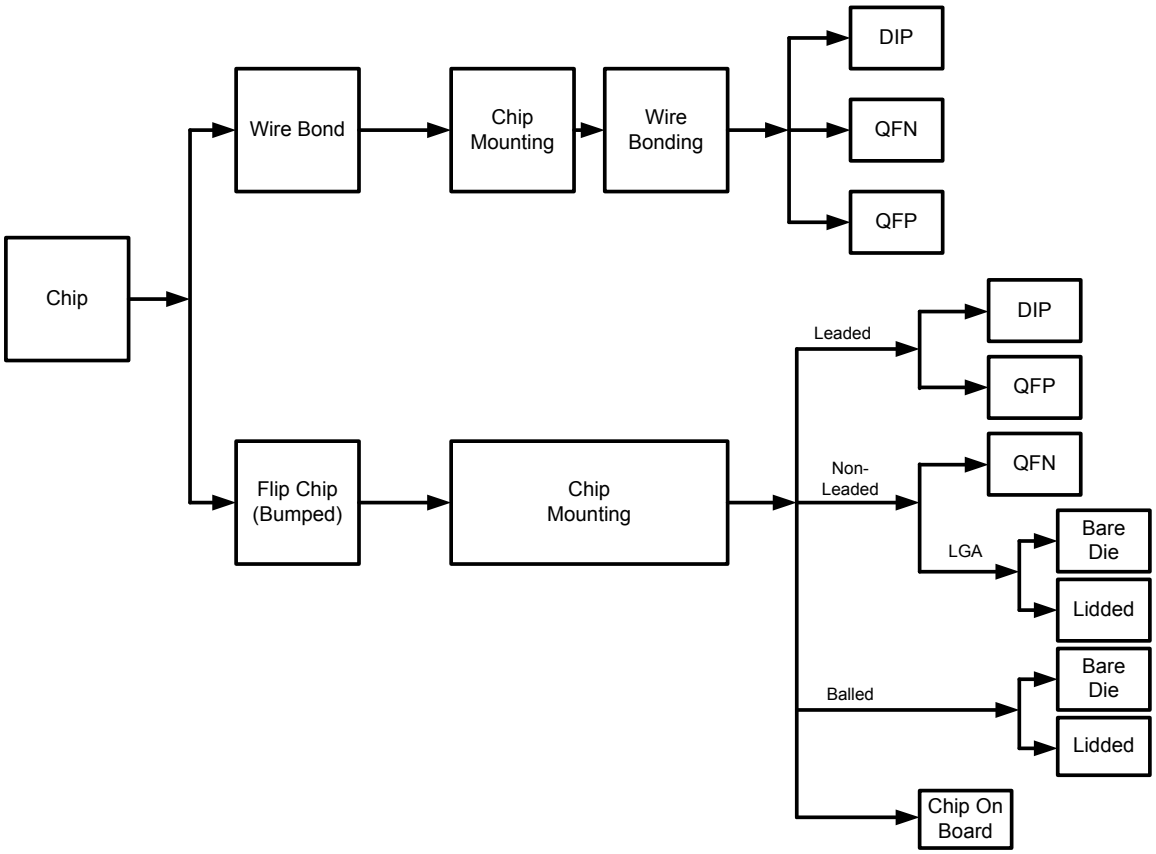
Figure 1 shows the process flow from bare chip to the chip mounted in a package. The package selection is primarily based on a number of factors:

- Electrical connection
  When packaging a WB chip, the number of electrical connections is relatively small (say less than 40) and package size is not critical, the DIP package is a good choice. It is easy to handle and is relatively mechanically rugged. The QFP is capable of more leads (i.e., connections) and the package height is comparable to the DIP. However, the QFP usually has a larger footprint in the X-Y dimensions. The QFN can be thinner and also have a larger number of connections. In large production volumes, the QFN is the cheapest package.

  FCs can have a lot more connections because the bumps can be arrayed across the entire chip surface. So the packages for this type of chip must also be capable of a large number of connections, thus usually ruling out the peripheral connection pack-

Thermal Test Chip Packaging (continued)

Figure 1



ages associated with WB chips. Of course, low bump-count FCs can also be mounted in peripheral packages. The most current most common high-connection count packages are the BGA and LGA (think of a BGA with out the balls) packages. Depending on the package size, ball/land size and ball/land pitch, several thousand connections are possible.

- Mechanical protection

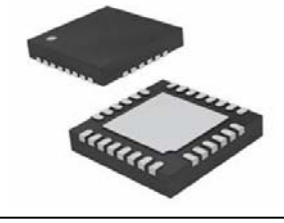
  Key duties of any package are to provide mechanical protection for the chip and physical connection to the chips electrical contacts. In a DIP, QFP or QFN, the chip is attached to a mounting area and then wire bonds are made between the package connection pads and the chip wire bond pads. The assembly is then molded over or sealed with a lid. Some QFN packages with properly designed lead frames accept a flip chip directly and are then molded over to seal the chip within the package. LGA and BGA packages have contact pads that match the bumps on the chip; these pads are electrically connected to the package lands or balls. The flip chip is attached using a reflow process, and then subjected to an underfill process that fills the voids around the bumps. If a lid is required, thermal interface material is introduced between the backside of the chip and the underside of the metal lid.

Thermal Test Chip Packaging (continued)

- Reliability requirements
  Package failures are induced by temperature, humidity, vibration, shock, pressure, electrical bias, EMI, and corrosive atmospheres. The end-use application determines the level of protection needed from these failure modes and what materials, processes and methods can be used to detect and then prevent early failure. A reliability plan is mandatory for all products and should be determined at the start of the product development cycle. Many standards exist from commercial, to military to aerospace.

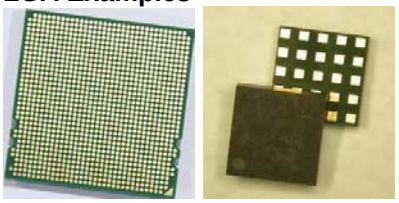
- Thermal management
  The best way to get heat from the chip out to the surrounding environment is via direct contact with the backside of the chip (as in a bare die LGA or BGA package) or with the chip directly attached to a mounting surface that becomes part of the package outside surface (referred to as a direct attach pad [DAP]). These approaches provide the lowest thermal resistance from the device junction on the chip to thermal interface surface – bare chip backside or DAP. Other package alternatives will usually have some material between the chip backside surface and the package surface that will impede heat flow.

QFN Examples

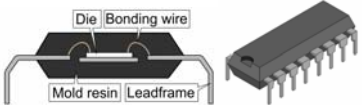


QFP Example

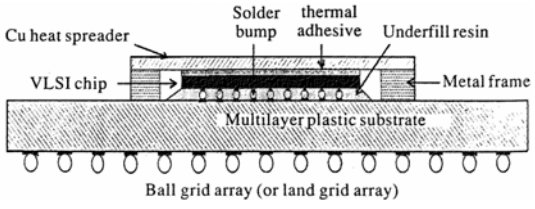
LGA Examples



DIP Examples



Lidded BGA Cross Section



Flip Chip BGA Example