THERMAL TEST CHIPS

TTC-1002

DESCRIPTION

The TTC-1002 thermal test chip is designed to provide a maximum of flexibility for thermal characterization of semiconductor packages. Each die can be used individually or in a square or rectangular array. Strategically placed diode temperature sensors enable temperature measurements to be made in the center, corner and mid-side of an individual die or any configuration array. All diodes, whether in a single die or arrayed die configuration, can be individually addressed, allowing for temperature contour measurements across a die or an array. The two heating resistors on each die can be powered individually or wired in a series or parallel configuration for operation from a single power supply. In an array configuration, there are several resistor series strings that can be individually powered from separate power supplies or paralleled for operation from a single supply. The multiple resistor design allows for thermal measurements with non-uniform heating across the die or array.

FEATURES

- **Multiple diode sensors for measurement of die temperature contours**
- **Multiple heating resistors for uniform and non-uniform heating setup**
- **Designed for square or rectangular array applications**
- **Kelvin connection for heating resistors to improve thermal measurement accuracy**
- **Multiple sizes to accommodate a wide range of package characterization requirements**
- **Supplied in wafer form, allowing for user-specific backside treatment**
- **Wafer designed with metal interconnection between die to eliminate inter-cell wire bond requirements**

SPECIFICATIONS

Electrical - Heating	TTC-1002
# of Resistors	2
Resistance Value	7.6 Ω ±10 % (each resistor)
Resistance Variation	±5 % (for die from a specific wafer)
Max Resistor Power	6 W (6V @ 1A) each
Connection	Force & Sense wire bond or bump pads
Resistor Coverage	>85% of die area within wire bond pads

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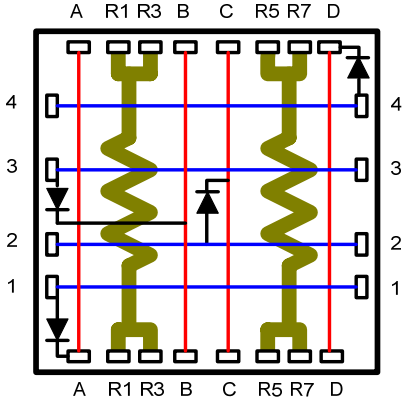
SPECIFICATIONS (continued)

Electrical - Sensing	TTC-1002
# of Diodes	4 (1 center, 2 opposing corners, 1 mid-side)
Nominal V_F	0.71 V @ I_F = 1 mA each diode
Nominal BV_R	7 V @ I_R = 10 µA each diode
Addressing	Row and Column wire bond or bump pads
Physical	
Die Size	2.54 X 2.54 mm (0.10 X 0.10 inch)
Die Layout	See Figure 1
Array Capability	See Figure 2
Array Size **(nominal)** - 2 X 2 (example of how wafer can be scribed) 3 X 3 4 X 4	**5.8** X 5.08 mm (0.20 X 0.20 inch) 7.64 X 7.64 mm (0.30 X 0.30 inch) **10.2** X 10.2 mm (0.40 X 0.40 inch)
Wafer Thickness	0.64 mm (0.025 inch) Nominal
Wafer Backside Finish	Ground, un-polished
Wire Bond Pad Size	Resistors - 0.20 X 0.15 mm (0.008 X 0.006 inch) Diodes - 0.1 X 0.1 mm (0.004 X .004inch)
Wafer Size	152 mm (6 inch) Diameter Nominal
Wafer Yield	Greater than 80%
Approximate Unit Cell Die/Wafer	>1200

Figure 1 Chip Layout



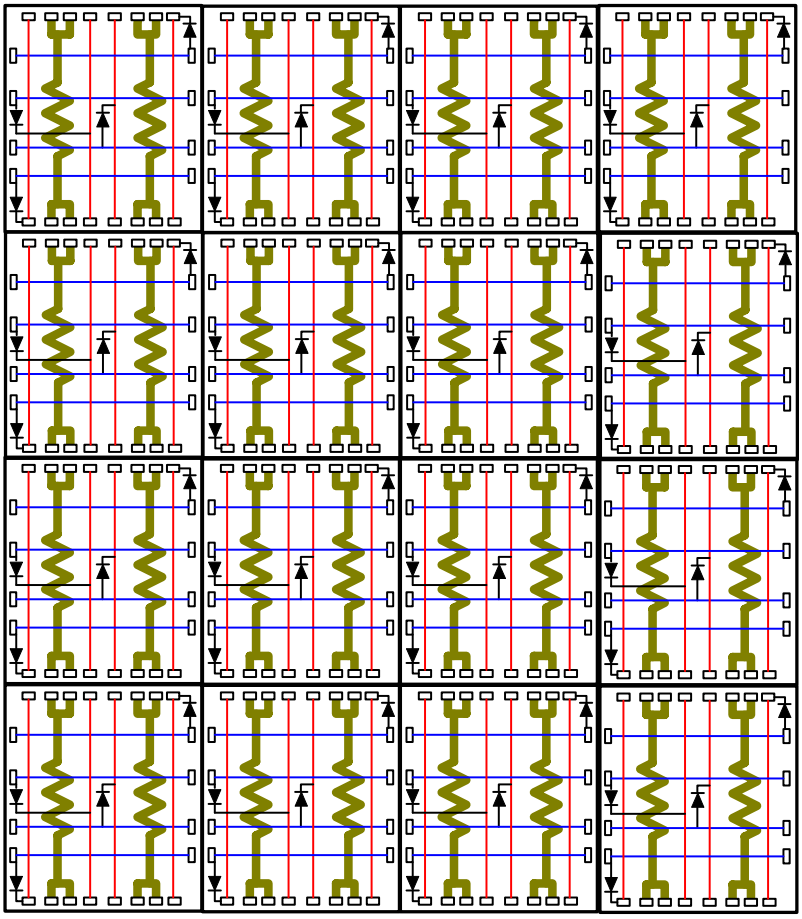


Figure 2 Typical Array Layout (Shown as 4 X 4 array)