NEW THERMAL TEST CHIP: MEETS JEDEC STANDARDS

FLEXIBLE AND HIGH PERFORMANCE THERMAL TEST CHIP NOW AVAILABLE

IEEE SEMI-THERM25 SYMPOSIUM, SAN JOSE, CA. — March 17, 2009 — Thermal Engineering Associates, Inc. (TEA) announces the immediate availability of a new thermal test chip, TTC-1002, that complies with standard EIA/JESD51-4 and is flexible enough to meet virtually all of the requirements for general purpose semiconductor thermal testing applications. Wafers and cell arrays may be ordered for wire bond or bump connection applications. Thermal test chips are widely used to eliminate electronics heat dissipation problems through package/system level thermal characterization, package assembly process optimization, and heat sink thermal solution evaluation.

Thermal test chips are semiconductor devices that can deliver precise thermal loads to specific geographic areas of a semiconductor package or printed circuit board (PCB) in order to simulate the thermal performance characteristics of the subsystem. Applications for thermal test chips include:

- Package thermal requirements testing
- Package thermal simulation and verification
- Package mechanical stress testing
- Power mapping of thermal effects
- PCB level thermal simulation
- System level thermal simulation

TEA founder and President, Bernie Siegal, has been supplying thermal test and measurement products and services for over 40 years. “Our new thermal test chip finally meets all JEDEC and general user requirements,” said Siegal, “I have worked very hard over the last 10 years to come up with a thermal test chip that is nearly perfect with regard to maximizing the heated area in each cell, uniformity of cell heating, easy access to strategically placed measurement diodes, accurate measurements, and flexibility in simulating the widest range of application specific semiconductors.”

The TTC-1002 is based upon a unit cell design in which a cell may be used individually or combined in a matrix of up to 40 x 40. Each cell is 2.5mm on a side and regardless of the size of the cell matrix, there is periphery access for all heating and Kelvin enabled measurement connections. Strategically placed diode sensors enable thermal measurements in the center, center periphery and all diagonals, regardless of the size or configuration of the cell array. Two individual metal film heating elements cover 87% of the die surface for uniform heating of each half of the cell, as needed. The two heating elements may be connected in series or in parallel.

- More -

Pricing and Availability:
Minimum wafer order is 2 and the price for 2-9 wafers is $3,550 each (wire bond), 2 to 13 weeks ARO. Unit cells and arrays may be purchased as well. Contact TEA for pricing detail.

About Thermal Engineering Associates:
TEA and its president, Bernie Siegal, have been providing thermal test and measurement hardware, software, and consulting services since 1973. Siegal has been chairman of the JEDEC JC15 committee and is the principle author of many MILSTD 750 thermal test methods. All major semiconductor companies, packaging companies, and many system level OEMs have utilized TEA equipment and/or services during its long history. Siegal is a founding member of IEEE SEMI-THERM and has delivered numerous papers and articles on thermal testing, simulation, and evaluation methods and techniques and is frequently sought out as a lecturer and expert in the field. www.thermeng.com.

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